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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,446	12/20/2001	Anthony Richard Huggett	MM-141	5357

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,446	HUGGETT ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the numerical references to the drawings must be removed. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites, “second dimension encoder means representative of n_x encoders”, which is indefinite since it is not clear what is meant by a single encoder “representative of n_x encoders”.

Claim 14 recites similar language as in claim 1.

Claim 2-13 and 15-26 depend from respective base claims 1 and 14; hence inherit the deficiencies of their respective base claims.

Claim 13 recites the limitation "the output counter" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 14, are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue).

35 U.S.C. 102(b) rejection of claims 1 and 14.

Inoue teaches a method of encoding a product code having a first dimension systematic block code of length n_x elements and a second dimension systematic block code of length n_y elements (n_x= n_2 and n_y= n_1 in Figure 4 of Inoue) including the steps of: a. applying a data element stream to first dimension encoder means to produce said first dimension systematic block code having k_x data elements and n_x-k_x parity elements, where said parity elements are derived from said k_x data elements (col. 1, lines 34-59 of Inoue teaches that the columns comprising k_x=k_2 bits are encoded by applying a data

element stream to first dimension C_2 encoder means of Figure 6A to produce said first dimension systematic block code having $k_x = k_2$ data elements and n_x-k_x,i.e., $n_2-k_2=m_2$, parity elements, where said parity elements are derived from said k_x data elements), b. repeatedly applying said data element stream to said first dimension encoder means to produce k_y first dimension code vectors, where k_y is the data element length of the second dimension systematic block code (col. 1, lines 34-59 of Inoue teaches that the C_2 encoder means of Figure 4 encodes the first dimension data symbols by repeatedly applying f times said data element stream to said first dimension C_2 encoder means of Figure 4 to produce $k_y = k_1$ first dimension code vectors, where $k_y = k_1$ is the data element length of the second dimension systematic block code), c. as each one of said k_y first dimension code vectors is produced, outputting said first dimension code vectors to second dimension encoder means representative of n_x encoders (the C_1 encoder means of Figure 4 of Inoue is a second dimension encoder means for receiving the first dimension encoded vectors and is representative of $n_x = n_2$ necessary to encode the $n_x = n_2$ rows of Figure 4 in Inoue), d. deriving $n_xn_y-n_xk_y$ parity elements for said second dimension systematic block code vectors (the C_1 encoder means of Figure 4 of Inoue produces $n_2n_1-n_2k_1=n_2(n_1-k_1)=n_x(n_y-k_y)= n_xn_y-n_xk_y$ parity elements), and e. outputting second dimension code vectors as each is produced so as to provide said encoded product code (Modulator 28 in Figure 6A is a device for outputting second dimension code vectors as each is produced so as to provide said encoded product code).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue) in view of Aitsab et al. (Aitsab, O.; Pyndiah, R.; Performance of Reed-Solomon block turbo code, GLOBECOM '96, Volume: 1, 18-22 Nov. 1996, Pages:121 – 125, hereafter referred to as Aitsab).

35 U.S.C. 103(a) rejection of claims 2 and 15.

Inoue substantially teaches the claimed invention described in claims 1 and 14 (as rejected above).

However Inoue does not explicitly teach the specific use of a product turbo code.

Aitsab, in an analogous art, teaches use of a product turbo code. Note: structurally, there is no difference between encoders for a product code and a turbo product code.

What makes any code into a turbo code is the decoding means and Aitsab teaches turbo decoding of a typical product code such as the one taught in Inoue.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inoue with the teachings of Aitsab by including use of a product turbo code. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a product turbo code would have provided the opportunity to increase coding gains (see Abstract, Aitsab).

4. Claims 3, 4, 13, 16, 17, 20, 21 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue).

35 U.S.C. 103(a) rejection of claims 3 and 16.
Inoue substantially teaches the claimed invention described in claims 1 and 14 (as rejected above).
However Inoue does not explicitly teach the specific use of n_x encoders.
The Examiner asserts that Inoue teaches a plurality of second dimension encoders, but does not specify an exact number for the encoders, hence use of n_x encoders is a specific embodiment encompassed by the teachings in the Inoue patent.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue by including use of n_x encoders.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of n_x encoders would have provided the opportunity to implement a specific embodiment encompassed by the teachings in the Inoue patent.

35 U.S.C. 103(a) rejection of claims 4 and 17.

Inoue substantially teaches the claimed invention described in claims 1, 3, 14 and 16 (as rejected above). In addition, Figure 11A and 11B in Inoue teaches a multitude of memory elements for implementing the n_x encoders.

However Inoue does not explicitly teach a specific means using RAM for implementing the n_x encoders.

The Examiner asserts that RAM is memory and that it would be an obvious engineering design choice to use RAM to implement the memory elements in Figures 11A and 11B of Inoue based on obvious engineering design choices such as available materials.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue by using RAM for implementing the n_x encoders. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using RAM for implementing the n_x encoders would have provided the opportunity to implement the memory elements in Figures 11A and 11B of Inoue based on obvious engineering design choices such as available materials.

35 U.S.C. 103(a) rejection of claims 13 and 26.

Inoue substantially teaches the claimed invention described in claims 1 and 14 (as rejected above). In addition, Inoue teaches a timing signal generator 24 in Figure 6A of Inoue for controlling and synchronizing the operation of encoding circuitry.

However, Inoue does not explicitly teach the specific details of circuitry for implementing the timing signal generator 24 of Figure 6A in Inoue.

The Examiner asserts that use of specific circuitry for implementing the timing signal generator 24 of Figure 6A in Inoue would be an obvious engineering design choice based on design requirements and available circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue by including the specific details of circuitry for implementing the timing signal generator 24 of Figure 6A in Inoue. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the specific details of circuitry for implementing the timing signal generator 24 of Figure 6A in Inoue would have provided the opportunity to implement the timing signal generator 24 of Figure 6A in Inoue based on obvious engineering design choice such as design requirements and available circuitry.

35 U.S.C. 103(a) rejection of claims 20 and 21.

If b=1 in Figure 4 of Inoue, then said data element is a single binary bit. If b>1, then said data element has a length of two or more binary digits.

35 U.S.C. 103(a) rejection of claims 27 and 28.

Inoue teaches a method of encoding a product code having a first dimension systematic block code of length n_x elements and a second dimension systematic block code of length n_y elements (n_x= n_2 and n_y= n_1 in Figure 4 of Inoue) including the steps of: a. applying a data element stream to first dimension encoder means to produce said first dimension systematic block code having k_x data elements and n_x-k_x parity elements, where said parity elements are derived from said k_x data elements (col. 1, lines 34-59 of Inoue teaches that the columns comprising k_x=k_2 bits are encoded by applying a data element stream to first dimension C_2 encoder means of Figure 6A to produce said first dimension systematic block code having k_x= k_2 data elements and n_x-k_x,i.e., n_2-k_2=m_2, parity elements, where said parity elements are derived from said k_x data elements), b. repeatedly applying said data element stream to said first dimension encoder means to produce k_y first dimension code vectors, where k_y is the data element length of the second dimension systematic block code (col. 1, lines 34-59 of Inoue teaches that the C_2 encoder means of Figure 4 encodes the first dimension data symbols by repeatedly applying f times said data element stream to said first dimension C_2 encoder means of Figure 4 to produce k_y= k_1 first dimension code vectors, where k_y= k_1 is the data element length of the second dimension systematic block code), c. as each one of said k_y first dimension code vectors is produced, outputting said first dimension code vectors to second dimension encoder means representative of n_x encoders (the C_1 encoder means of Figure 4 of Inoue is a second dimension encoder means for receiving the first

dimension encoded vectors and is representative of $n_x = n_2$ necessary to encode the $n_x = n_2$ rows of Figure 4 in Inoue), d. deriving $n_x n_y - n_x k_y$ parity elements for said second dimension systematic block code vectors (the C_1 encoder means of Figure 4 of Inoue produces $n_2 n_1 - n_2 k_1 = n_2(n_1 - k_1) = n_x(n_y - k_y) = n_x n_y - n_x k_y$ parity elements), and e. outputting second dimension code vectors as each is produced so as to provide said encoded product code (Modulator 28 in Figure 6A is a device for outputting second dimension code vectors as each is produced so as to provide said encoded product code). In addition, Inoue teaches a plurality of second dimension encoders, but does not specify an exact number for the encoders, hence use of n_x encoders is a specific embodiment encompassed by the teachings in the Inoue patent. Adtionally, Figure 11A and 11B in Inoue teaches a multitude of memory elements for implementing the n_x encoders. However Inoue does not explicitly teach a specific means using RAM for implementing the n_x encoders.

The Examiner asserts that RAM is memory and that it would be an obvious engineering design choice to use RAM to implement the memory elements in Figures 11A and 11B of Inoue based on obvious engineering design choices such as available materials. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue by using RAM for implementing the n_x encoders. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using RAM for implementing the n_x encoders would have

provided the opportunity to implement the memory elements in Figures 11A and 11B of Inoue based on obvious engineering design choices such as available materials.

5. Claims 5-12, 18, 19 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue) in view of Yu et al. (Nam Yul Yu; Young Kim; Pil Joong Lee; Iterative decoding of product codes composed of extended Hamming codes, Proceedings Fifth IEEE Symposium on Computers and Communications, 3-6 July 2000, Pages: 732 - 737).

35 U.S.C. 103(a) rejection of claims 5, 6, 9-12, 18, 19 and 22-25.
Inoue substantially teaches the claimed invention described in claims 1 and 14 (as rejected above).
However Inoue does not explicitly teach the specific use of a Hamming product code. Yu, in an analogous art, teaches a Hamming product code. The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have been highly motivated to use Hamming codes since Hamming codes simplify decoding. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inoue with the teachings of Yu by including use of a Hamming product code. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a Hamming product code would have provided the opportunity to simplify decoding.

35 U.S.C. 103(a) rejection of claims 7 and 8.

If b=1 in Figure 4 of Inoue, then said data element is a single binary bit. If b>1, then said data element has a length of two or more binary digits.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hladik; Stephen Michael et al. (US 5734962 A) teaches serially concatenated inner and outer encoders whereby the outer encoder is comprised of parallel concatenated constituent encoders for use in a turbo encoder. Picart, A.; Pyndiah, R.; Performance of turbo-decoded product codes used in multilevel coding, Conference Record, IEEE International Conference on Communications Converging Technologies for Tomorrow's Applications, Volume: 1, 23-27 June 1996 Pages: 107 – 111.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133